In the Specification

Please amend paragraph **[0004]** as shown:

Bitline BLA and another bitline BLB of the DRAM form a pair of bitlines coupled to a sense amplifier 15. The other bitline BLB of the pair~~, which~~ is not coupled to a memory cell 10A accessed by the activated wordline WLA, but is instead coupled to a memory cell 10B which is only accessible by a different wordline WLB. Bitline BLB retains a bitline precharge voltage, and is used to provide a reference voltage to a sense amplifier 15~~ to which BLA is also connected~~. At the sense amplifier 15, the small voltage difference between BLA and BLB of the bitline pair is amplified to rail-to-rail logic levels. The amplified logic level signals on the bitline pair BLA, BLB are then available to be read out from the memory. If the particular column address corresponding to bitline BLA has been selected through column select line CSL, the signals on the bitline pair are transferred to a pair of data lines DLA and DLB.

Please amend paragraph **[0036]** as shown:

After a period of delay, determined in relation to the RASP strobe signal, the row control circuitry 130 generates the wordline interlock signal 132, which is then provided to X-decoders of the RWL decoder 106, and results in the deactivation of the RWL 114. Since the wordline interlock signal 132 is provided directly to each X-decoder 200, it disables the X-decoder regardless of the state of the precharge signal X_PRE 134, or the respective states of the address inputs Xij, Xkl, Xmn. The timing of

the wordline interlock signal 132 is preferably controlled by the row control circuitry 130 in a manner which provides a timing margin relative to the SETN signal which times the start of signal amplification by the sense amplifiers 120. Thus, in a preferred embodiment, after a read wordline 114 is activated, ~~after which~~ data from gain cells accessed thereby are sensed by the sense amplifiers 120 upon receiving the SETN signal. ~~, and the~~ The sensed data is then latched by data latch circuitry 124 to hold the read data ready for data transfer. After these events, the row control circuitry 130 activates the wordline interlock signal 132, in response to which the RWL is deactivated. In this way, the read wordlines of the gain cell array are operated with a shortened "ON" time, or "active" time that is ended by the wordline interlock signal 132. Thereafter, the precharge cycle is promptly begun, to prepare for the next read operation.

Please amend paragraphs **[0040]** and **[0041]** as shown:

The bitline monitor interlock signal 322 is also used by row control circuitry 330 to generate a SETN signal to time the activation of sense amplifiers 326, after which the data is latched by data latch circuitry 324. The row control circuitry 330 also uses the bitline monitor interlock signal 322 ~~and~~ to generate a bitline precharge signal (BPRE 308) at a short time thereafter, this signal being input to bitline precharge circuitry 323. As also shown in Figure 3a, the bitline monitor interlock signal 322 is also provided to a circuit 340 which generates the row address strobe signal (RASP) as a way of providing overriding control over the cycle time of the gain cell DRAM 300. By monitoring the timing of the bitline monitor interlock signal 322 over time, the RASP

generator 340 can determine if the read cycle time of the DRAM can be decreased, as by shortening the intervals between RASP signals.

In response to the bitline monitor interlock signal 322 the address buffer 350 is also disabled, causing address inputs Xi and Xib to predecoder 352 to be returned to the precharge state. This is performed in order to prevent oscillation through the closed loop then existing through the X-decoder ~~200~~ inside the RWL decoder 306, RWL driver 307 and bitline monitoring circuitry 310 and 312.

Please amend paragraph **[0047]** as shown:

As further illustrated in Figure 5b, while holding the RASP signal and an external row address strobe (RAS) signal active at the input to row control circuitry 530, a read command to a single read address is issued to initiate read cycle operation. As in the example shown in Figure 3a, the read row address (ADD) is decoded by predecoder 552 and RWL decoder 506 to activate a RWL 502 of the array 500 by RWL driver 507, in turn. The signal on the sample read bitline (RBL) 520 is then monitored by the bitline monitoring circuitry 510 and when it reaches a sufficient magnitude, the bitline monitor interlock signal (INTLOCK) 522 is generated. The bitline monitor interlock signal (INTLOCK) 522, as provided to RWL decoder 506, then disables the X-decoder therein, such that the RWL 514 is deactivated. Bitline precharge (BPRE) and sense amplifier

set signals (SETN) are triggered in response to the bitline monitor interlock 522. The BPRE signal is input to the bitline precharge circuitry 523, and the SETN is input to the sense amplifiers 526. The output of the sense amplifiers is latched by data latch circuitry 524.